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EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2111	12

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/825,818	Applicant(s) VOGT ET AL.	
	Examiner Thomas J. Cleary	Art Unit 2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-15 and 17-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 17-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 10, 11, 12, 13, 14, 15, 17, 18, 19, 20, 21, 22, 23, 24, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 6,502,156 to Sacker et al. ("Sacker"), US Patent Number 4,586,128 to DeWoskin ("DeWoskin"), and US Patent Number 5,430,676 to Ware et al. ("Ware").

3. In reference to Claim 10, Sacker teaches providing one or more expansion slots configured to receive a respective add-in card including a processor thereon (See Figure 2 and Column 2 Lines 49-57), generating a signal indicative of the presence of said add-in card in one of the expansion slots (See Figure 2 and Column 3 Lines 26-32), and non-intermittently masking a host device select signal generally used by said host to assert control of a controller on the motherboard of said host in response to said signal indicative of the presence of said add-in card (See Figure 2, Column 1 Lines 31-43 and Column 3 Lines 29-32). Sacker does not teach imparting a predefined time

delay to a bus grant signal configured to grant control rights to the processor on said add-in card, in lieu of said host, over said controller, wherein said time delay corresponds to a clocking cycle of a clocking signal for said electrical bus; and propagating said bus grant signal to said controller upon completion of said clocking cycle and the signal indicative of the presence of said add-in card actually indicating the presence of said add-in card in one of the expansion slots, thereby propagating said bus grant signal synchronously with the clocking signal for said electrical bus for effecting the control rights of said processor over said controller. DeWoskin teaches a grant signal used to grant control rights to a controller, which is equivalent to the processor of Claim 10, to access a memory interface, which is equivalent to the controller of Claim 10 (See Abstract and Column 1 Lines 32-56). Ware teaches imparting a predefined time delay of one clock cycle onto a control signal, which is equivalent to the bus grant signal, and propagating said signal synchronously with the clocking signal (See Column 8 Line 62 – Column 9 Line 23).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Sacker with the arbitrator of DeWoskin and the programmable delay of Ware, resulting in the inventions of Claim 10, in order to prevent both bus masters, which are equivalent to the host controller and first peer device, from simultaneously taking control of the second peer device (See Column 1 Lines 20-23 of DeWoskin); and to allow the latency of the control signal to be set and therefore help to maximize the bandwidth utilization of the bus (See Column 8 Lines 58-66 and Column 9 Lines 21-23 of Ware).

4. In reference to Claim 11, Sacker, DeWoskin, and Ware teach the limitations as applied to Claim 10 above. Sacker further teaches a PCI bus (See Column 2 Lines 30-35).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Sacker with the arbitrator of DeWoskin and the programmable delay of Ware, resulting in the inventions of Claim 11, in order to prevent both bus masters, which are equivalent to the host controller and first peer device, from simultaneously taking control of the second peer device (See Column 1 Lines 20-23 of DeWoskin); and to allow the latency of the control signal to be set and therefore help to maximize the bandwidth utilization of the bus (See Column 8 Lines 58-66 and Column 9 Lines 21-23 of Ware).

5. In reference to Claim 12, Sacker, DeWoskin, and Ware teach the limitations as applied to Claim 11 above. Sacker further teaches that a RAID processor is located on an add-in card (See Figure 2 and Column 2 Lines 49-57).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Sacker with the arbitrator of DeWoskin and the programmable delay of Ware, resulting in the inventions of Claim 12, in order to prevent both bus masters, which are equivalent to the host controller and first peer device, from simultaneously taking control of the second peer device (See Column 1 Lines 20-23 of DeWoskin); and to allow the latency of the control signal to be set and

therefore help to maximize the bandwidth utilization of the bus (See Column 8 Lines 58-66 and Column 9 Lines 21-23 of Ware).

6. In reference to Claim 13, Sacker, DeWoskin, and Ware teach the limitations as applied to Claim 12 above. Sacker further teaches that the controller on the motherboard of the host comprises an I/O controller (See Column 1 Lines 41-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Sacker with the arbitrator of DeWoskin and the programmable delay of Ware, resulting in the inventions of Claim 13, in order to prevent both bus masters, which are equivalent to the host controller and first peer device, from simultaneously taking control of the second peer device (See Column 1 Lines 20-23 of DeWoskin); and to allow the latency of the control signal to be set and therefore help to maximize the bandwidth utilization of the bus (See Column 8 Lines 58-66 and Column 9 Lines 21-23 of Ware).

7. In reference to Claim 14, Sacker, DeWoskin, and Ware teach the limitations as applied to Claim 10 above and further teaches passing the host device select signal from the host to the controller in the absence of said add-in card (See Figure 2 and Column 3 Lines 29-32).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Sacker with the arbitrator of DeWoskin and the programmable delay of Ware, resulting in the inventions of Claim 14, in order to

prevent both bus masters, which are equivalent to the host controller and first peer device, from simultaneously taking control of the second peer device (See Column 1 Lines 20-23 of DeWoskin); and to allow the latency of the control signal to be set and therefore help to maximize the bandwidth utilization of the bus (See Column 8 Lines 58-66 and Column 9 Lines 21-23 of Ware).

8. In reference to Claim 15, Sacker teaches a computer host coupled to first and second peer devices by a common bus (See Figures 1 and 2 and Column 2 Lines 24-48), a generating module configured to supply a signal indicating the presence of a first peer device (Figure 2 Number 40 and Column 3 Lines 26-41), and a hiding module configured to non-intermittently hide a second peer device from the host so that the second peer device is controlled by the first peer device whenever the signal indicates the presence of the first peer device (See Figure 2 Numbers 42 and 43 and Column 3 Lines 26-32), wherein said hiding module comprises a masking module coupled to receive said signal indicative of the presence of said first device to mask a host device select signal generally supplied by the host to said second peer device. Sacker does not teach a delay device for imparting a predefined time delay to a bus grant signal configured to grant control rights to the first peer device, in lieu of said host, over said second peer device, wherein said time delay corresponds to a clocking cycle of a clocking signal for said electrical bus, said delay device electrically coupled to propagate said bus grant signal to said second peer device upon completion of said clocking cycle and the signal indicative of the presence of the first peer device actually

indicating the presence of said first device, thereby propagating said bus grant signal synchronously with the clocking signal for said electrical bus for effecting the control rights of said first peer device over said second peer device. DeWoskin teaches a grant signal used to grant control rights to a controller, which is equivalent to the first peer device of Claim 15, to access a memory interface, which is equivalent to the second peer device of Claim 15 (See Abstract and Column 1 Lines 32-56). Ware teaches imparting a predefined time delay of one clock cycle onto a control signal, which is equivalent to the bus grant signal, and propagating said signal synchronously with the clocking signal (See Column 8 Line 62 – Column 9 Line 23).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Sacker with the arbitrator of DeWoskin and the programmable delay of Ware, resulting in the inventions of Claim 15, in order to prevent both bus masters, which are equivalent to the host controller and first peer device, from simultaneously taking control of the second peer device (See Column 1 Lines 20-23 of DeWoskin); and to allow the latency of the control signal to be set and therefore help to maximize the bandwidth utilization of the bus (See Column 8 Lines 58-66 and Column 9 Lines 21-23 of Ware).

9. In reference to Claim 17, Sacker, DeWoskin, and Ware teach the limitations as applied to Claim 15 above. Sacker further teaches a PCI bus (See Column 2 Lines 30-35).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Sacker with the arbitrator of DeWoskin and the programmable delay of Ware, resulting in the inventions of Claim 17, in order to prevent both bus masters, which are equivalent to the host controller and first peer device, from simultaneously taking control of the second peer device (See Column 1 Lines 20-23 of DeWoskin); and to allow the latency of the control signal to be set and therefore help to maximize the bandwidth utilization of the bus (See Column 8 Lines 58-66 and Column 9 Lines 21-23 of Ware).

10. In reference to Claim 18, Sacker, DeWoskin, and Ware teach the limitations as applied to Claim 17 above. Sacker further teaches that the HBA, which comprises a processor, can enhance a SCSI device to allow it to perform RAID functions, and thus inherently functions as a RAID processor (See Figure 2 and Column 2 Lines 55-57).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Sacker with the arbitrator of DeWoskin and the programmable delay of Ware, resulting in the inventions of Claim 18, in order to prevent both bus masters, which are equivalent to the host controller and first peer device, from simultaneously taking control of the second peer device (See Column 1 Lines 20-23 of DeWoskin); and to allow the latency of the control signal to be set and therefore help to maximize the bandwidth utilization of the bus (See Column 8 Lines 58-66 and Column 9 Lines 21-23 of Ware).

11. In reference to Claim 19, Sacker, DeWoskin, and Ware teach the limitations as applied to Claim 18 above. Sacker further teaches a Zero Channel RAID adapter. Since Zero Channel RAID requires an I/O controller provided in the motherboard of the circuitry to interface with the I/O device it is inherent that there is a motherboard mounted I/O controller working with the I/O device taught by Sacker (See Figure 2 and Column 1 Lines 31-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Sacker with the arbitrator of DeWoskin and the programmable delay of Ware, resulting in the inventions of Claim 19, in order to prevent both bus masters, which are equivalent to the host controller and first peer device, from simultaneously taking control of the second peer device (See Column 1 Lines 20-23 of DeWoskin); and to allow the latency of the control signal to be set and therefore help to maximize the bandwidth utilization of the bus (See Column 8 Lines 58-66 and Column 9 Lines 21-23 of Ware).

12. In reference to Claim 20, Sacker, DeWoskin, and Ware teach the limitations as applied to Claim 19 above. Sacker further teaches that the I/O controller is mounted in the motherboard of the host (See Column 1 Lines 41-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Sacker with the arbitrator of DeWoskin and the programmable delay of Ware, resulting in the inventions of Claim 20, in order to prevent both bus masters, which are equivalent to the host controller and first peer

device, from simultaneously taking control of the second peer device (See Column 1 Lines 20-23 of DeWoskin); and to allow the latency of the control signal to be set and therefore help to maximize the bandwidth utilization of the bus (See Column 8 Lines 58-66 and Column 9 Lines 21-23 of Ware).

13. In reference to Claim 21, Sacker, DeWoskin, and Ware teach the limitations as applied to Claim 20 above. Sacker further teaches the RAID processor is located on an add-in card (See Figure 2 and Column 2 Lines 49-57).

One of ordinary skill in the art at the time the invention was made would combine the device of Sacker with the arbitrator of DeWoskin and the programmable delay of Ware, resulting in the inventions of Claim 21, in order to prevent both bus masters, which are equivalent to the host controller and first peer device, from simultaneously taking control of the second peer device (See Column 1 Lines 20-23 of DeWoskin); and to allow the latency of the control signal to be set and therefore help to maximize the bandwidth utilization of the bus (See Column 8 Lines 58-66 and Column 9 Lines 21-23 of Ware).

14. In reference to Claim 22, Sacker, DeWoskin, and Ware teach the limitations as applied to Claim 15 above. Sacker further teaches that the select signal from the host device is passed to the second peer device in the absence of the first peer device, since the absence of the card means the signal is not driven low and therefore does not turn off the switch (See Figure 2 and Column 3 Lines 26-32).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Sacker with the arbitrator of DeWoskin and the programmable delay of Ware, resulting in the inventions of Claim 22, in order to prevent both bus masters, which are equivalent to the host controller and first peer device, from simultaneously taking control of the second peer device (See Column 1 Lines 20-23 of DeWoskin); and to allow the latency of the control signal to be set and therefore help to maximize the bandwidth utilization of the bus (See Column 8 Lines 58-66 and Column 9 Lines 21-23 of Ware).

15. In reference to Claim 23, Sacker, DeWoskin, and Ware teach the limitations as applied to Claim 16 above. Ware further teaches that the delay device comprises a flip-flop (See Figure 17 Number 530 and Column 9 Lines 9-10).

One of ordinary skill in the art at the time the invention was made would combine the device of Sacker with the arbitrator of DeWoskin and the programmable delay of Ware, resulting in the inventions of Claim 23, in order to prevent both bus masters, which are equivalent to the host controller and first peer device, from simultaneously taking control of the second peer device (See Column 1 Lines 20-23 of DeWoskin); and to allow the latency of the control signal to be set and therefore help to maximize the bandwidth utilization of the bus (See Column 8 Lines 58-66 and Column 9 Lines 21-23 of Ware).

16. In reference to Claim 24, Sacker, DeWoskin, and Ware teach the limitations as applied to Claim 16 above. Sacker further teaches that the masking module is comprised of a plurality of switches. The masking module equivalent circuitry of Sacker comprises two inverter logic gates and a transistor switch (See Figure 2 Numbers 42 and 43 of Sacker). Since each inverter logic gate is inherently comprised of at least one switching device, said circuitry comprises a plurality of switching devices.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Sacker with the arbitrator of DeWoskin and the programmable delay of Ware, resulting in the inventions of Claim 24, in order to prevent both bus masters, which are equivalent to the host controller and first peer device, from simultaneously taking control of the second peer device (See Column 1 Lines 20-23 of DeWoskin); and to allow the latency of the control signal to be set and therefore help to maximize the bandwidth utilization of the bus (See Column 8 Lines 58-66 and Column 9 Lines 21-23 of Ware).

17. In reference to Claim 25, Sacker, DeWoskin, and Ware teach the limitations as applied to Claim 16 above. Sacker further teaches that the masking module is comprised of a plurality of logic gates. The masking module equivalent circuitry of Sacker comprises two inverter logic gates and a transistor switch (See Figure 2 Numbers 42 and 43 of Sacker).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Sacker with the arbitrator of DeWoskin

and the programmable delay of Ware, resulting in the inventions of Claim 24, in order to prevent both bus masters, which are equivalent to the host controller and first peer device, from simultaneously taking control of the second peer device (See Column 1 Lines 20-23 of DeWoskin); and to allow the latency of the control signal to be set and therefore help to maximize the bandwidth utilization of the bus (See Column 8 Lines 58-66 and Column 9 Lines 21-23 of Ware).

Drawings

18. The drawings were received on 31 March 2004. These drawings are acceptable.

Response to Arguments

19. Applicant's arguments filed 31 March 2004 with respect to Claims 10-15 and 17-25 have been fully considered but are moot in view of the new ground(s) of rejection. Applicant has significantly modified the scope of the claims, and as shown above, such changes are not persuasive to overcome a rejection based on 35 USC §103. The new ground(s) of rejection presented in this Office action in reference to the aforementioned claims have been necessitated by the Applicant's amendment.

20. Applicant has argued that the device of Sacker masks the host device select signal intermittently. In the device of Sacker, the host device select signal is identified

as 'AD[11+x+n]', which is shown passing through masking switch 43 and connected to 'IDSEL' of I/O Device 26. When HBA 34 is present in slot 30, signal 'TMS' is driven low, thereby turning off masking switch 43 and preventing the host device select signal from passing through (See Column 3 Lines 27-33). Signal 'TMS' remains low until HBA 34 is removed from slot 30, and which point signal 'TMS' is pulled high, thereby turning on masking switch 43 and allowing the host device select signal to pass through. Because signal 'TMS' remains low at all times while an HBA 34 is in slot 30, masking switch 43 remains off during that entire time, and thus non-intermittently masks the host device select signal.

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent Number 5,812,858 to Nookala et al. ("Nookala") and US Patent Number 5,835,733 to Walsh et al. ("Walsh") were received from Applicant in response to a notification that copies of said prior art, which were listed on an Information Disclosure Statement filed by Applicant, were not received.

22. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The examiner can normally be reached on Monday-Thursday (7-4), Alt. Fridays (7-3).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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